

**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

13. (Currently Amended) A method for fabricating a ferroelectric random access memory (FRAM) device comprising:

- a) forming a lower electrode;
- b) forming a lower seed layer on the lower electrode;
- c) forming a ferroelectric layer on the lower seed layer by one of a sputtering or a CVD process;
- d) forming on the ferroelectric layer an upper seed layer for forming a Perovskite crystal structure of the ferroelectric layer;
- e) annealing the resultant structure of steps a) through d), including completing the perovskite crystal structure of the ferroelectric layer; and
- f) forming an upper electrode on the upper seed layer.

14. (Original) The method according to claim 13, wherein forming a ferroelectric layer comprises forming a PZT ferroelectric layer on the lower seed layer.

15. (Original) The method according to claim 13, wherein the forming the upper and lower seed layers includes using a material having a crystallization temperature lower than that of a material for forming the ferroelectric layer.

16. (Previously Presented) The method according to claim 13, wherein forming the upper and lower seed layers includes using a ferroelectric material having a same lattice constant as that of a material for forming the ferroelectric layer.

17. (Original) The method according to claim 14, wherein the forming the upper and lower seed layers includes using  $\text{PbTiO}_3$ ,  $\text{TiO}_2$  or PZT having at least one of a higher Pb content and a higher Ti composition ratio than a PZT to be used to form the ferroelectric layer.

18. (Original) The method according to claim 13, wherein the forming the lower electrode and the upper electrode includes using a Pt-group metal layer, a conductive oxide layer or a dual layer of the Pt-group metal layer and the conductive oxide layer.

19. (Previously Presented) The method according to claim 13, further comprising, prior to forming the lower electrode, forming a switching element to be electrically connected to the lower electrode.

20. (Previously Presented) The method according to claim 13, further comprising:

before forming the lower electrode

providing a semiconductor substrate; and

forming a gate insulating layer on the semiconductor substrate, and

after forming the upper electrode

forming source and drain regions in a portion of the semiconductor substrate adjacent to a periphery of the gate insulating layer.